**Assignments on Basic gates**

1. AND gate

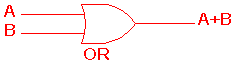
Symbol:

|  |  |  |  |
| --- | --- | --- | --- |
| http://electrosofts.com/verilog/and.jpg  Truth table: | | | |
|
| **A** | **B** | **Y** | |
| 0 | 0 | 0 | |
| 0 | 1 | 0 | |
| 1 | 0 | 0 | |
| 1 | 1 | 1 | |

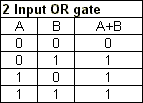
y = a & b;

**OR GATE:**

Symbol:

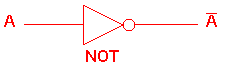


Truth table:



**NOT GATE:**

Symbol:

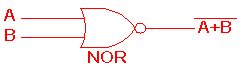


Truth table:

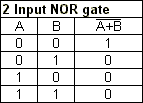


**NOR GATE:**

Symbol:

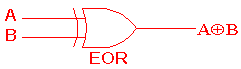


Truth table:

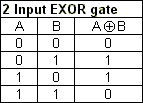


**XOR GATE:**

Symbol:

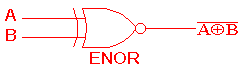


Truth table:

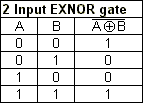


**XNOR GATE:**

Symbol:

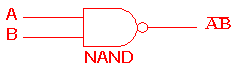
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Truth table:

****

**NAND GATE:**

Symbol:



Truth table:

